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Research Paper

RESULT PAPER: LOW NOISE AMPLIFICATION CMOS TECHNIQUE

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ABSTRACT

The wireless communication industry is currently experiencing tremendous growth. In responding to the demand for a low-cost but high performance wireless front-end, many intensive researches on CMOS radio-frequency (RF) front-end circuits have been carried out. The ultimate goal is to minimize the trade-off between high performance and low-cost, low power consumption design. Low noise amplifier (LNA) is typically the first stage of a receiver. Its performance greatly affects the overall receiver performance. In this thesis, four LNAs are proposed. They are designed for the IEEE 802.15.4 standard in the 2.4 GHz ISM band. The first three LNAs are optimized for low NF and low power. An application of this type of LNA is to be used as the amplification stage before the active mixer in the receiver chain. Active mixer provides active gain while consuming some dc power. Therefore, high LNA gain is required in this type of system. There is one important contribution in this research. Firstly, LNA (LNA1) that combining the merits of the inductive source degeneration common-source LNA (L-CSLNA) and the common-gate LNA (CGLNA) is introduced. The proposed LNA1 is a fully differential -boosting CGLNA with series inductor input matching network that improves the NF. The circuit's input matching, NF and gain have been derived to verify the design methodology. The LNA was designed and fabricated using 0.18 µm CMOS technology. It consumes only 0.98 mA from 1.0 V power supply and achieves a measured gain of 15 dB and NF of 5 dB. The series inductor input matching CGLNA is attractive for low-power fully integrated applications in CMOS technologies. Even though the high NF problem of the CGLNA has been addressed in the proposedLNA1, we wish to further reduce the NF to achieve better trade-off between NF and power consumption.

KEYWORDS

CMOS LNA, CGLNA

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1. INTRODUCTION

LNA needs to be matched to the output of the filter following the antenna to prevent the incoming signal from reflecting back and forth between the LNA and the antenna. While the LNA is a relatively simple design compared to other RF components in a cellular receiver chain, the performance tradeoffs challenge the LNA design engineer. LNA design typically involves making choices between directly competing performance parameters such as: noise, gain, linearity and power consumption. In the IEEE 802.15.4 standard, the NF and linearity requirement can be relaxed in order to achieve other important parameters such as gain and power.

1.1.OBJECTIVE AND MAJOR CONTRIBUTIONS

The objectives of our research are to develop a thorough understanding of low-power LNA design and to introduce new low-power LNA design for the IEEE 802.15.4 standard. , four LNAs are proposed for the 2.4 GHz ISM band of IEEE802.15.4 standard. The first three LNAs were optimized for low NF and low power consumption while the fourth LNA was optimized for high gain. The first design (LNA1) is a fully differential -boosting CGLNA with series inductor input matching network that retains the advantages of both the CSLNA and CGLNA topology. It consumes only 0.9 mA from 1.0 V power supply and achieves a measured gain of 15 dB and NF of 5 dB.

In the second design (LNA2), we introduced a noise cancellation technique that reduces the NF of the CGLNA to achieve better trade-off between NF and power consumption. The LNA achieves a measured gain of 14.8 dB, NF of 4.5 dB and IIP3 of -5.7dBm respectively. It consumes only 0.95mW from 1.0 V supply voltage. The third LNA (LNA3) was designed with low supply voltage to reduce the total power consumption. LNA3 was designed to operate at 0.6 V supply voltage.

It uses a single-stage non-cascode structure with CCC across the two sides of a differential input stage. The CCC technique had been employed in many other LNAs. However, it was mainly used to improve the LNA‟s NF and none of the LNAs using CCC had demonstrated low voltage operation properly. In this work, the CCC technique is not only used to lower the LNA‟s NF, but also to improve the reverse isolation of the single-stage non-cascode structure. A novel analysis on the feedback cancellation mechanism of the CCC technique was carried out. At 2.4 GHz, it has an input matching better than -24 dB and a reverse isolation better than -38 dB; produces 14 dB gain and 3.55 dB NF while drawing only 0.83 mA current from a 0.6 V supply voltage. The fourth LNA (LNA4) was designed to achieve very high gain. The π-match and capacitive feedback input network were utilized. The capacitive feedback network helps to save on chip area by using only one inductor for the input matching. The π-match network

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introduces an additional degree of design freedom and allows the LNA to achieve higher gain than the conventional L-CSLNA. It achieves a gain of 21.7 dB with a S11 of -12 dB while consuming only 0.6 mW. The NF is 4.9 dB. For all designs, the circuit's input matching, noise factor and gain have been derived to verify the design methodology. Compared to recent related works, our LNAs consume the least power but still achieve a very good performance in other parameters.

1.2 PERFORMANCE TRADE-OFFS IN LNA DESIGN

Different application has different requirement for LNA performance. Therefore, it is important to understand the trade-offs involved in LNA design. The three important trade-offs are gain vs. power efficiency, linearity vs. drain-source dc current and LNA's gain vs. receiver's dynamic range.

Gain vs Power efficiency

As we all know, an amplifier's gain is proportional to the trans-conductance, gm, of its input transistor. High gm is desirable for high gain. Using the standard saturation region dc current equations for long channel devices,

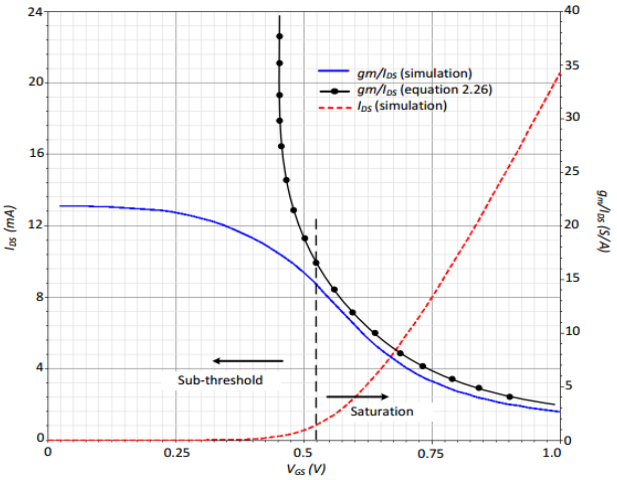

Figure 1: Variation of *IDS* and *gm/IDS* with *VGS* in CSM 0.18 µm RF CMOS technology (W=120 µm)

As seen in Figure 1, gm/IDS the calculated based on equation is fairly close to the simulation one for Vg greater than.0.55 V The ratio doesn't approach infinity for which is 0.45 V in our simulation. This is because equation (2.26) is only applicable for the transistor in saturation region. In sub-threshold region, the MOSFET behavior is similar to a BJT, therefore is nearly constant

The analysis and simulation results clearly demonstrate the trade-off between gain and power efficiency. High gain but low power efficiency is achieved at high while high power efficiency but low gain is achieved at low

1 .3 THE PROPOSED SERIES INPUT RESONANCE CGLNA (LNA1)

LNA1 combined the series RLC input matching network of the L-CSLNA with the CGLNA topology. The RLC input network adds an additional degree of freedom to the input matching design and improves the NF of the CGLNA. These advantages will be presented below.

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1.4 INPUT MATCHING

Figure 2 and 3 shows the schematic of LNA1 and its equivalent small signal circuit for input matching analysis.

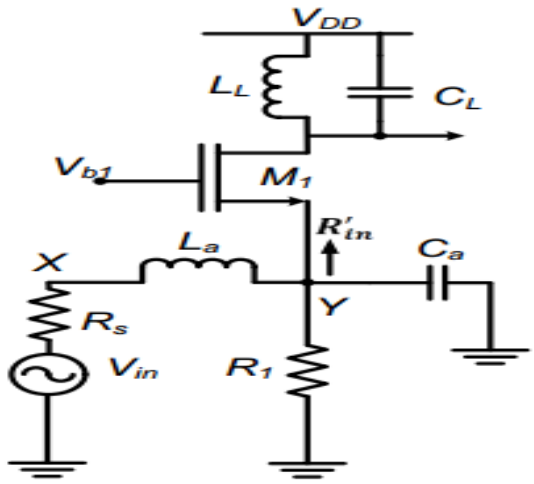

Figure 2 The proposed CGLNA with series input matching Noise analysis

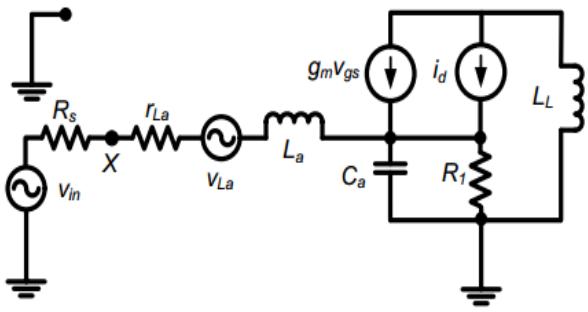

Figure 3. Noise analysis small signal model of LNA1

The small signal model shown in Figure 3 is used to derive the NF of this LNA. In the noise analysis, the effect of gate noise is omitted since its contribution to the total NF is negligible compared to other noise sources. The noise factor of the conventional CGLNA including the effect of R1 and Ca is:

$$F_{CGLNA} = 1 + \beta_1 \cdot \frac{\gamma}{\alpha} \frac{g_m}{R_s} \cdot \left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_P}{1 + g_m r_{ds}}}{1 + g_m R_s + (R_s + R_P)\frac{1}{r_{ds}}} \right)^2$$

$$+ \beta_1 \cdot \frac{r_{LL}}{R_s} \cdot \left(\frac{R_s + \frac{1}{1/r_{ds} + g_m} + \frac{R_P}{1 + g_m r_{ds}}}{1 + g_m R_s + (R_s + R_P)\frac{1}{r_{ds}}} \right)^2 + \frac{R_s}{R_1}$$

If R1=infinite, and Ca=0, then B1 (beta) which is consistent The NF simulation results are shown in Figure 4. Our CGLNA with series input matching achieves much lower NF than the conventional CGLNA. By adding the series inductor La, the noise contribution from the channel thermal noise is reduced resulting in a lower NF of LNA1. The simulation results agree well with the analysis. There is a great improvement of NF. When Gm is at its lowest value which is 6 mS in our simulation, the NF improvement is up to 1.2 dB.

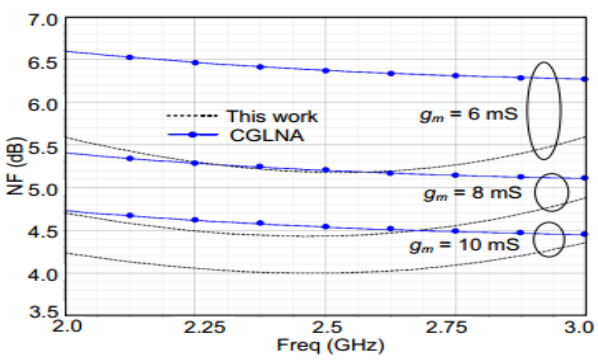

Figure 4: Simulated NF versus different *gm* values in the 0.18µm RF CMOS technology

2 . CIRCUIT IMPLEMENTATION

To demonstrate the idea, an LNA was designed and fabricated in a standard 0.18 µm RF CMOS technology. To further improve the gain performance of the circuit, two big capacitors Cc were placed across the two sides of a differential

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input stage to effectively boost the transistor's trans conductance value without requiring extra dc current. The use of Cc introduced an inverting amplification, A, at the source and the gate terminal of the input device.

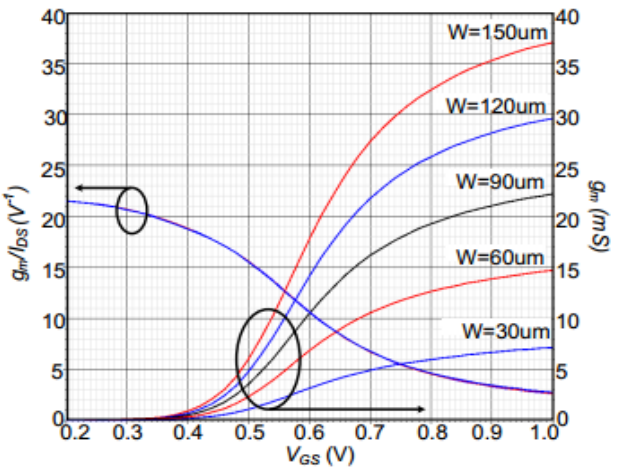

Figure 5: Variation of *gm* and *gm* /*IDS* with *VGS* and transistor size in the 0.18 µm RF CMOS technology

The Gm value of the input transistor is chosen based on the gain requirement. Figure 7 plots this ratio vs transistor size at 2.4 GHz. In our simulation, the highest value occurs when the transistor width is 150 µ

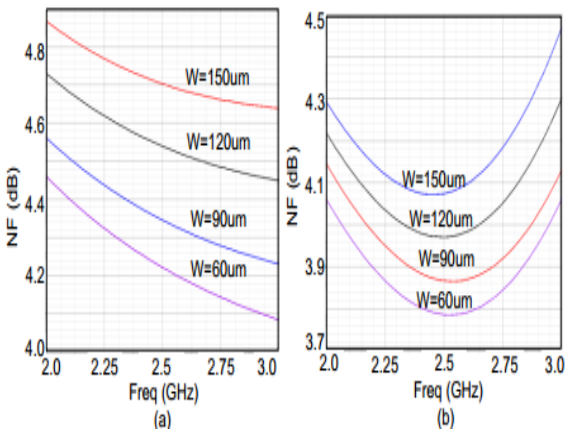

Figure .6: Simulated NF versus different transistor sizes at *gm* =10 mS in the 0.18 µm RF CMOS technology (a) CGLNA (b) LNA1

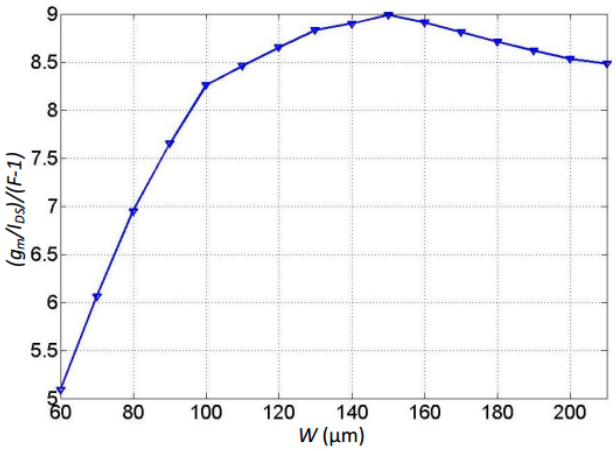

Figure 7: LNA1 vs transistor size at 2.4 GHz and *gm* =10 mS in the 0.18 µm RF CMOS technology

The schematic and chip micrograph of LNA1 is shown in Figure 3.8. The LNA was designed using standard Vth transistors, metal-insulator-metal (MIM) capacitors, and standard spiral inductors

3 MEASUREMENT RESULTS AND DISCUSSION

The measurement setup is shown in Figure 3.9. The LNAs are measured using the HP8510 Network analyzer which has a built-in NF personality. The measurement is based on RF-probing. The basic test setup includes a wafer probe station, the HP8510 network analyzer system and a bias supply. The network analyzer consists of a sweep synthesizer (so that measurements will be repeatable), a test set which includes two ports, a control panel, an information display, and two RF cables to hook up the design-under test (DUT). Each port of the test set includes dual directional couplers and a complex ratio measuring device.

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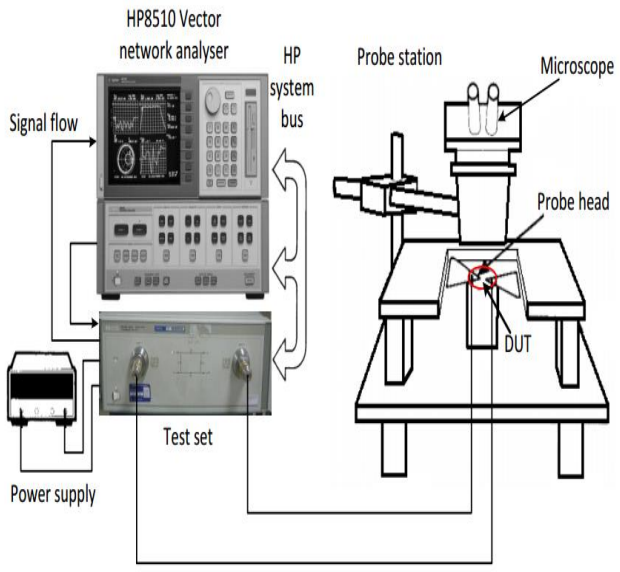

Figure 8: Measurement set-up

A test signal is generated by the signal generator (from the network analyzer). The test set takes the signal generator output and routes it to the DUT and it routes the signal to be measured back to the receiver of the network analyzer. The receiver makes the measurements. A network analyzer will have one or more receivers connected to its test ports. This set-up was used for the measurement of all four LNAs. Figure 3.10 shows the measured *S11* and *S21* of LNA1. The LNA has better than -10 dB input matching over the desired band. At 2.4 GHz, the voltage gain is 15 dB. Figure 7 shows the measured and simulated NF of the LNA. The measured NF exceeded the simulated NF by 1dB. This difference can be attributed to the poor noise modeling and process variation. At 2.4 GHz, the measured NF is 5 dB.

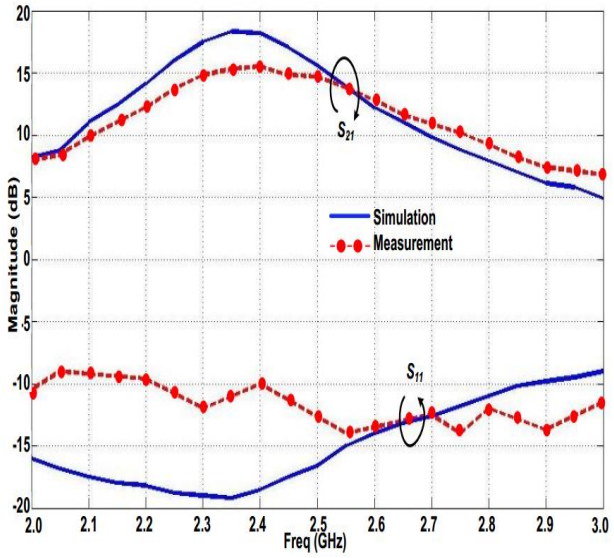

Figure 10: Measured and simulated *S11* and *S21* of LNA1

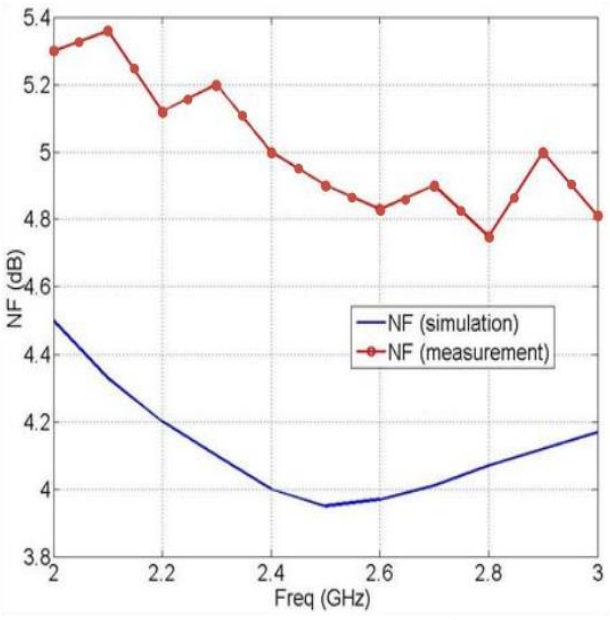

Figure 11: Measured and simulated NF of LNA1

Figure 12 shows the *S12* and stability factor *K* and Δ. For an LNA to be stable, *K* and Δ must be larger and smaller than unity respectively. LNA1 has high reverse isolation and is stable at the frequency of interest as seen on Figure 12. (*S12* = -63 dBm, *K*>1 and Δ<1at 2.4 GHz). The LNA core only consumes 0.98 mW power from 1.0 V supply voltage, making it suitable for low-power applications. The measured *IIP3* of the LNA core is -19 dBm. The use of resistor at the source of transistor *M1a* and *M2a* together with the low

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supply voltage at 1.0 V has limited the linearity performance of this LNA. LNA1's performance is summarized in Table 2.

The comparisons of this LNA with recently published 2.4 GHz LNAs and state-of the-art ultra-low power LNAs are summarized in Table 1. Two figures of merits (FOM) [91] are used to compare the performance of the LNAs. The *FOM1* is a function of the operating frequency, gain, noise factor, and power consumption.

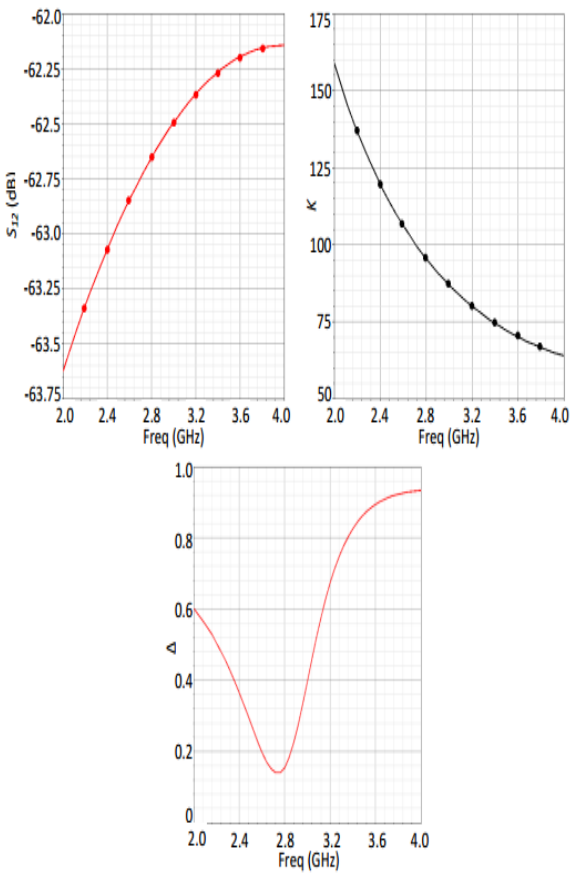

Figure 12: *S12* , *K* and Δ of LNA1

Table 1: LNA1's measurement results

LNA's Specification	Requirement	Measurement results
Gain	15 dB	15 dB
NF	< 16.19 dB	5 dB
IIP3	> -19.77 dBm	-15 dBm
S_{11}	< -10 dB	-11 dB
S_{12}	< -30 dB	-63 dB

The LNAs in [30, 43, 92, 93] have better NF but consume much more power than ours. Moreover, such low NF is not necessary for our application. The works in [21] and **[77]** have better FOM than ours. Both designs bias the transistors in sub-threshold region for high power efficiency. [21] Has good FOM due to its high gain of 21.4 dB which is achieved by using large resistive load. Therefore, it can't operate at low supply voltage such as 1.0 V. **[77]** achieves the best FOM due to its low supply voltage (0.6 V). However, it has low gain of 9.1 dB. This is due to the small inductive load of 2 nH. Our *FOM2* is low due to the low *IIP3*. In order to improve the *FOM2*, in the next designs we will increase the linearity. To improve the *FOM1*, we will reduce the NF, increase gain or reduce the power consumption. In this, an ultra-low power sub-mA series input resonance with –boosting technique differential CGLNA was presented. The design methodology was explained, the proposed LNA was fabricated and its performance was compared with other works. Unlike the conventional CGLNA, the value of this LNA is not fixed by the input matching condition which makes optimizing for low power possible.

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	[77]	[95]	[21]	[30]	[92]	[93]	[43]	LNA1
Tech (nm)	130	130	180	130	130	130	90	180
Freq (GHz)	3.0	5.1	2.4					
Pdc (mW)	0.4	1.03	1.13	6.5	17	3.2	3	0.98
Gain (dB)	9.1	10.3	21.4	13	10	16.5	15	15
NF (dB)	4.7	5.3	5.2	3.6	3.7	2.66	3	5.0
S_{11} (dB)	-17	-17.7	-19	-14	-25	-11.8	-30	-11
IIP3 (dBm)	-11	n/a	-11	n/a	-6.7	-4.93	-7	-19
V_{DD} (V)	0.6	0.4	1.8	1.2	1.2	1.2	0.6	1
FOM1 (dB)	10.4	8.32	10.33	1.07	-4.7	7.73	6.55	8.04
FOM2 (dB)	-0.6	n/a	-0.67	n/a	-11.49	2.8	-0.4	-10.96

Table 2: LNA1's performance comparisons

The LNA consumes only 0.98 mA from 1.0 V supply voltage and attains a measured NF of 5.0 dB and gain of 15 dB at 2.4 GHz. The LNA shows excellent trade-off between NF and power consumption. The measured power consumption is among the lowest in current literature. The proposed technique makes the CG topology attractive for low-power fully integrated designs.

CONCLUSION

The poor reverse isolation problem in the single-stage non-cascode structure is improved by employing the capacitive cross-coupling (CCC) across the two sides of a differential input stage. Out of the three LNAs Firstly, while we have covered and explored deeply on the topic of LNA, other important blocks such as mixer, post-mixer baseband amplifier, channel-select filter, analog to-digital converter, and frequency synthesizer should be designed. The study on system level design for the IEEE 802.15.4 standard therefore should be deeply investigated. We believe that significantly power consumption can be saved by further

exploring the performance trade-offs in the IEEE 802.15.4 standard.

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