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TFET MEMORY IN REDUCED POWER MODE

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ABSTRACT:

In this thesis, an integrated model with TFET devices and CMOS devices is pro- posed. The goal is to minimize static power as well as dynamic power in comparison to a CMOS only system. The analysis of the integrated model is conducted using Cadence Virtuoso Schematic L-Editing, Analog Design Environment and Spectre Circuit Simulator tools using the 20nm GaN TFET model and the 45nm CMOS free PDK device obtained from North Carolina State University. The experiment is confined to the schematic stage as the GaN TFET devices do not have layout cells or design rules which are required for fabrication, and post post-Silicon validation.

KEYWORDS:

CMOS DEVICES, FINFETS, BIPOLAR JUNCTION TRANSISTORS, TFETs.

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INTRODUCTION

Current research into VLSI design at the sub-micron technology level is facing issues due to leakage current, supply voltage and a subthreshold swing of CMOS devices. The leakage current is the unwanted current when the transistor is switched-off. Sup- ply voltage scaling helps with reducing dynamic power consumption. The subthresh- old swing shows the switching speed of the transistor at the linear operating region of the transistor and the leakage in the subthreshold region of the transistor.

Researchers have pursued various approaches to address the above issues includ- ing using nanotechnology materials and devices, seeking higher levels of integration, higher switching speed, and minimum power consumption. FinFET devices were pursued in order to integrate larger number of transistors on a chip at lower oper- ating voltages. The advantages of FinFETs include low body effects, the need for a single additional mask during fabrication, lower leakage current and lower threshold voltage. The disadvantage of these devices include the corner effect and the para- sitic source/drain resistance which lead to lower drive current [9]. Since the level of integration, the power consumption, and the switching speed are related to the device geometry and the ability to use interconnects with very small cross-section, nanotechnology materials (e.g., graphene or carbon nanotubes) were pursued. These materials can be incorporated into the devices to provide much shorter interconnect materials and very short channels.

TFET is a relatively new type of transistor which is similar to the popular CMOS transistor but with its source and drain doped of opposite type. TFETs are becoming increasingly popular in micro and nanoelectronic applications due to their consider- ably low static leakage when the transistor is turned-off compared to the CMOS transistors. As a result of this low leakage property, TFETs are being explored in various areas where power optimization is a primary concern including memory cells and non-critical logic paths.

CMOS transistors have been popular since the 1970s. However, they are known to consume energy while switching between ON and OFF operation states. CMOS are similar to the Bipolar Junction Transistors (BJTs) in that they both control the flow of current by raising and

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lowering energy barriers. The electrons flow from the source of the transistor to the drain through the channel formed in the bulk material substrate at the appropriate gate bias. The electrons flow through the conduction band and the holes flow through the lower energy valence band.

CIRCUIT AND RESULT DISCUSSION

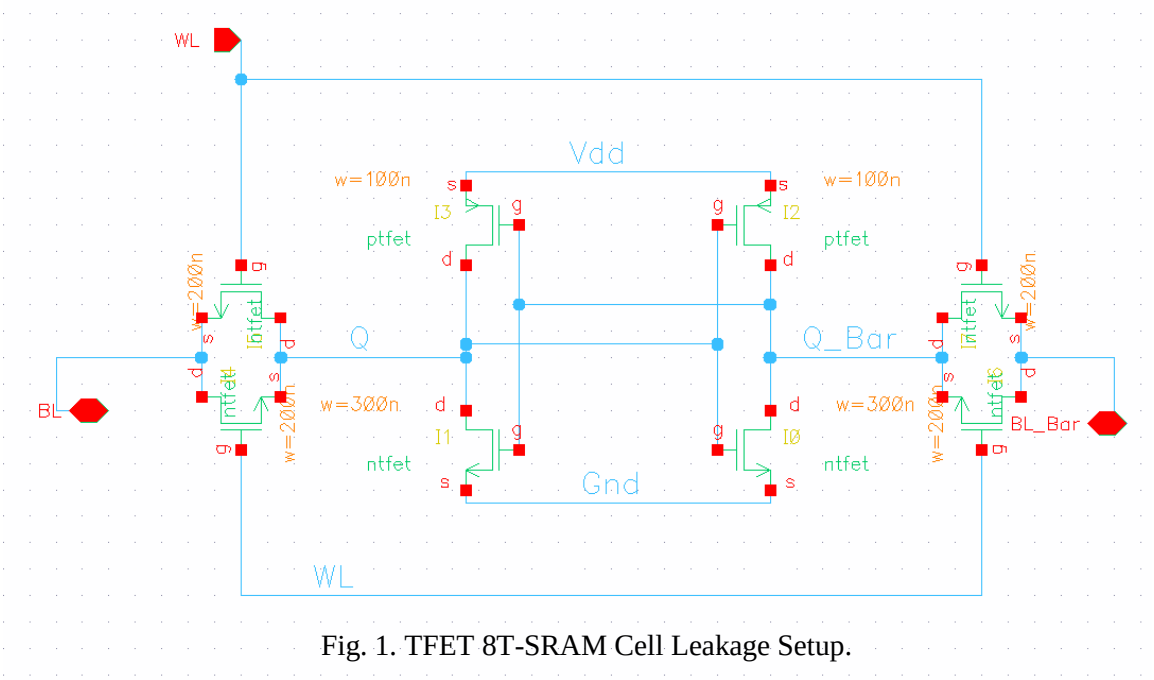

Fig. 1. TFET 8T-SRAM Cell Leakage Setup.

Table 1. Leakage Current and Static Power in SRAM Bitcells.

Device	L (nm)	W (nm)			Q (V)	I_{OFF} (nA)	P_{STATIC} (nW)
		PUN	PDN	Access			
TFET GaN	20	100	300	200	0	1.72	1.07
CMOS 45nm	45	225	675	450	0.6	30.2	18.1
CMOS 100nm	100	500	1500	1000	0	51.3	30.8

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CONCLUSION:

The designs in this thesis are limited to the schematic level. Future work, when layout cells and design rules can be obtained, will expanded to the physical level. The ability to conduct the analysis at the physical level may allow fabrication and post-silicon analysis which can in turn lead to more detailed assessments. The proposed design approach can also be investigated for lower level memories such the L2 cache or main memories. Theoretically, the longer the memory is switched-off, the more leakage current is dissipated from the memory arrays. Hence, using TFETs in lower level memories could be more advantageous than in upper-levels. In addition, the slower speed of TFETs could be less of an issue in lower-level memories when compared to upper-level memories.

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