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ANALYSIS OF UWB LNA IN 1GHZ-5GHZ RANGE USING CG INPUT STAGE

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ABSTRACT:

This paper presents a inductor-less broadband low-noise amplifier (LNA) implemented in 0.13 μm CMOS technology. The LNA use a CG input stage for wideband impedance matching, followed by two common source parallel amplifiers which perform distortion and noise cancellation. The LNA maintains minimum internal gain, noise figure at a given suply. While the LNA itself likewise adds some noise to the got signal, it is essential that this LNA infused noise is as least as conceivable to congratulate appropriate recovery of the signal in the later phases of the framework. Commonly because of the confinements in the execution of ADC it works at a lower frequency extend practically identical to the input RF go, in this manner one needs a blender to down proselyte the got RF signal.

KEYWORDS:

ADC, CAPACITOR, CG INPUT, CMOS TECHNOLOGY .

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INTRODUCTION

Wireless correspondence applications are hugely advancing. Innumerable escalated investigations on CMOS radio frequency (RF) front end circuits are being completed, in react to the interest for a low power and low expense with superior remote front end. The low-noise amplifier (LNA) is a basic square in the beneficiary chain used to amplify frail signals without including a great deal of noise, as the name suggests. By utilizing a LNA, the general result of noise figure coming about because of the consequent phases of the beneficiary chain can be limited by having sufficient addition of the LNA. While the LNA itself likewise adds some noise to the got signal, it is essential that this LNA infused noise is as least as conceivable to congratulate appropriate recovery of the signal in the later phases of the framework [1].

Fig. 1.1 speaks to the simplified square chart of a RF Narrow-Band Receiver [2] [6]. A radio wire is available as a first square it gets the input message signal. The band select channel is utilized to choose the ideal narrow bandwidth from the signal gotten by the recieving wire. A LNA at that point amplifies the separated low dimension input signal. The amplified signal may comprise unfortunate frequency segments due to the non-direct segments of the LNA. Commonly because of the confinements in the execution of ADC it works at a lower frequency extend practically identical to the input RF go, in this manner one needs a blender to down proselyte the got RF signal. Along these lines, the high Radio Frequency sifted signal is then down changed over into a middle of the road frequency with the guide of a nearby oscillator and a blender so as to encourage the activity of the analog to digital converter (ADC). This is additionally alluded to as demodulation. The digital signal processor is then used to process the IF or Base-Band signal.

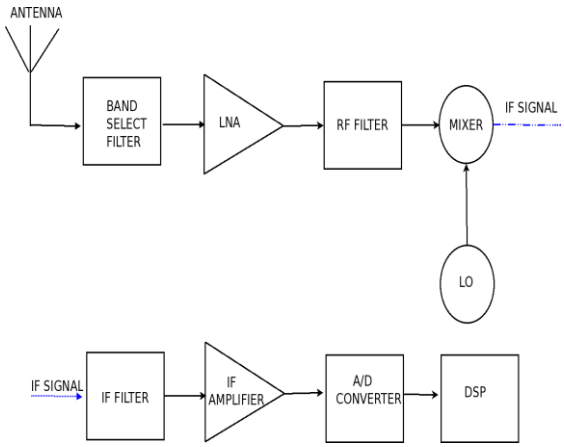

Figure 1.1: Simplified Narrow-Band RF Receiver

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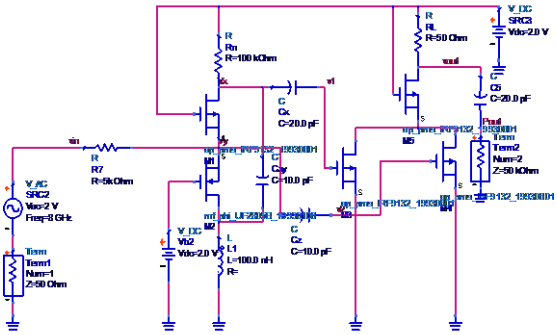
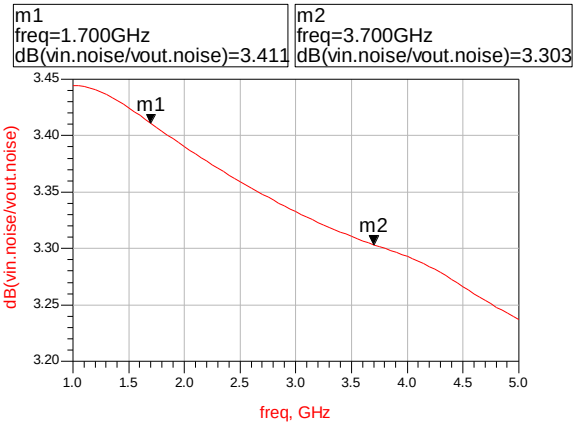
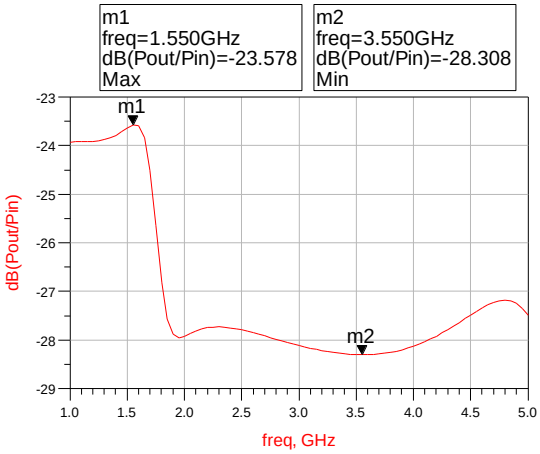
PROPOSED CIRCUIT



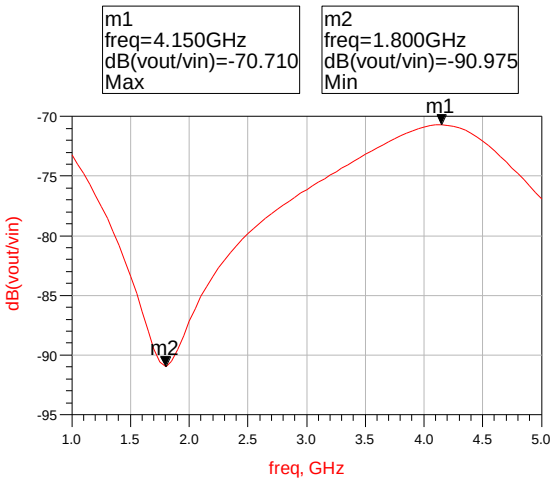
NOISE FIGURE



POWER GAIN



VOLTAGE GAIN



CONCLUSION:

A reconfigurable dual band LNA was designed to operate in 1 GHz and 5 GHz frequency bands. This design methodology is straight forward and it can be extended to other standards of operation. Due to the fact that the inductors are reused, the total design area would be relatively minimized as inductors generally requires a large fraction of chip area compared to transistors and capacitors. The LNA presented has the ability to operate in 1 GHz and 5 GHz frequency bands by simply enabling or disabling the control voltage V_c while avoiding any tuning mechanism at the input stage.

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